REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 19, and 49 have been amended. Claims 3, 5-6, 9-10, 21, 23-24, 27-28, and 50 were previously withdrawn. Claims 1-13, 15, 17, 19-31, 33, 35, and 49-50 are pending and under consideration.

A corrected drawing sheet labeled "Replacement Sheet" is submitted herewith and includes Figures 19-20, which have been labeled "Prior Art" as required by the Exmainer.

I. Rejections under 35 U.S.C. § 112

In the Office Action, at pages 2-3, claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35 and 49 were rejected under the first paragraph of 35 USC § 112 as failing to comply with the written description requirement. This rejection is respectfully traversed. The Examiner takes the position that the disclosure as originally filed fails to provide support for the limitation "forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value." This is incorrect.

Figs. 1-3 of the drawings each clearly illustrate a flowchart in which a displacement between a design position of an electronic component and the actual position of the electronic component on a board is calculated prior to forming vias in the board. Furthermore, page 10, line 3 through page 11, line 37 of the specification clearly discloses a process for forming a component-embedded board. Beginning at page 11, line 2, the specification states:

> Then, the displacement of the actual position of the electronic component 22-1 formed on the surface of the board 21 is calculated relative to the design position of the electronic component 22-1 that can be obtained from the design data.

The specification follows, at page 11, line 15:

> Furthermore, a maximum value may be predetermined for the displacement data with which the dynamic correction described later can be performed, and provisions may be made to **render the board defective if the displacement data exceeds the maximum value**. This serves to further increase the fabrication yield, because seriously defective parts that cannot be remedied by the dynamic correction **can be completely eliminated**

(**emphasis** added).

Then, the specification adds, beginning at page 11, line 34:

> Next, a via hole 25 for forming a via is formed in the insulating layer 23-1, as shown in Figure 6d. The via hole 25 is formed so as to expose the electrode portion 31 of the electronic component 22-1.

As such, the specification clearly supports the limitation "forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value," cited in claim 1, for example. One of ordinary skill in the art would clearly appreciate that the via holes are formed in the board only if the displacement does not exceed the predetermined maximum value because the specification clearly states that seriously defective parts that cannot be remedied by the dynamic correction can be completely eliminated, thus eliminating the need for continuing the fabrication process, which includes the further step of forming via holes.

In the Office Action, at page 3, claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35 and 49 were rejected under the second paragraph of 35 USC § 112 as being indefinite.

Independent claims 1, 19, and 49 have been amended in response to these rejections. The remaining claims depend from claims 1 and 19. Accordingly, withdrawal of these § 112 rejections is respectfully requested.

II. Rejections under 35 U.S.C. § 103

In the Office Action, at pages 3-6, claims 1-2, 4, 7-8, 11-13, 15, 17, 19-20, 22, 25-26, 29-31, 33, 35 and 49 were rejected under 35 USC § 103(a) as being unpatentable over Taff et al. (U.S. Patent No. 6,165,658) in view of Leedy (U.S. Patent No. 5,103,557).

Taff et al. and Leedy, alone or in combination, do not discuss or suggest:

> determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective; and
>
> correcting, based on said first displacement data, design data to be used for processing said board, covering said board with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value,

as recited in claim 1. Claim 1 provides for determining whether the displacement value between a design position and an actual position exceeds a predetermined maximum value at which the

board is rendered defective. Thereafter, claim 1 provides for performing corrections on design data to be used for processing the board only if the displacement value does not exceed the predetermined maximum value. Subsequent to performing corrections on the design data, claim 1 provides for covering the board with the first insulating layer to form a wiring pattern connected to the first electrical component and for forming via holes in the first insulating layer in accordance with the corrected design data. As such, the covering and forming are also performed only when the displacement value does not exceed the predetermined maximum value. In this manner, the invention of claim 1 serves to further increase the fabrication yield because seriously defective parts that cannot be remedied by the correction process can be completely eliminated and not further processed, thus saving unnecessary processing time.

The Examiner indicates that Taff et al. discloses the above discussed features of claim 1 at col. 8, lines 29-45. However, this is submitted to be incorrect. Taff et al. discloses determining the difference between the locations of conductive site 12 and conductive site 24, which are located on successive layers of a multi-layer PCB. However, Taff et al. merely discloses a preferred accuracy for the determined difference between the two conductive sites and further provides for correcting the determined difference regardless of the amount or degree of the difference. Taff et al. does not provide for determining whether or not the difference exceeds a predetermined maximum value (exceeds the preferred accuracy percentage) at which the PCB is rendered defective and correcting design data to be used for processing said board, covering the board with a first insulating layer to form a wiring pattern connected to a first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value. Taff et al. has no provision or criteria for rendering a board defective. Leedy fails to make up for these deficiencies in Taff et al.

Since Taff et al. and Leedy, either alone or in combination, do not disclose these features of claim 1, claim 1 patentably distinguishes over Taff et al. and Leedy. Accordingly, withdrawal of this § 103(a) rejection is respectfully requested.

Claims 2, 4, 7-8, 11-13, 15, and 17 depend either directly or indirectly from claim 1, and include all the features of claim 1, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 2, 4, 7-8, 11-13, 15, and 17 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

Taff et al. and Leedy, alone or in combination, do not discuss or suggest:

> determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective; and
>
> correcting, based on said first displacement data, design data to be used for processing said board, covering said board with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data only if the represented displacement does not exceed the predetermined maximum value,

as recited in claim 19, so that claim 19 patentably distinguishes over Taff et al. and Leedy. Accordingly, withdrawal of this § 103(a) rejection is respectfully requested.

Claims 20, 22, 25-26, 29-31, 33, and 35 depend either directly or indirectly from claim 19, and include all the features of claim 19, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 20, 22, 25-26, 29-31, 33, and 35 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

Taff et al. and Leedy, alone or in combination, do not discuss or suggest:

> means for determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective; and
>
> means for correcting, based on said first displacement data, design data to be used for processing said board, covering said board with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data, only if the represented displacement does not exceed the predetermined maximum value,

as recited in claim 49, so that claim 49 patentably distinguishes over Taff et al. and Leedy. Accordingly, withdrawal of this § 103(a) rejection is respectfully requested.

III. Interview Request

Applicants respectfully request a telephone interview between Applicants' representative, the undersigned, and the Examiner at the Examiner's earliest convenience, in order to discuss the arguments presented in the current response. The undersigned can be reached by telephone directly at (202) 454-1583.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 7-8-09

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